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8 APR 2003

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1. Your reference — P3166 GB PRO

2. Patent application number *(The Patent Office will fill in this part)* — 0308082.7

3. Full name, address and postcode of the or of each applicant *(underline all surnames)* — AOTI OPERATING COMPANY, INC.
131 NW HAWTHORNE AVENUE
SUITE 207
BEND, OREGON 97701, US

Patents ADP number *(if you know it)* — 8113805002

If the applicant is a corporate body, give the country/state of its incorporation — DELAWARE, USA

4. Title of the invention — OVERLAY ALIGNMENT MARK

5. Name of your agent *(if you have one)* — NOVAGRAAF PATENTS LIMITED

"Address for service" in the United Kingdom to which all correspondence should be sent *(including the postcode)* — THE CRESCENT
54 BLOSSOM STREET
YORK YO24 1AP

Patents ADP number *(if you know it)* — 08299166001 ✓

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Country	Priority application number *(if you know it)*	Date of filing *(day / month / year)*

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Number of earlier application	Date of filing *(day / month / year)*

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Any other documents *(please specify)*	

11. I/We request the grant of a patent on the basis of this application.

Signature NOVAGRAAF PATENTS LIMITED Date 08/04/2003

12. Name and daytime telephone number of person to contact in the United Kingdom PETER WILSON (DR) 01904 610586

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Overlay Alignment Mark

The invention relates to overlay metrology during semiconductor device fabrication, and in particular to an overlay alignment mark to facilitate alignment and/ or measure the alignment error of two layers on a semiconductor wafer structure, or different exposures on the same layer, during its fabrication.

Modern semiconductor devices, such as integrated circuits, are typically fabricated from wafers of semiconductor material. In particular, a wafer is fabricated comprising a succession of patterned layers of semiconductor material.

Overlay metrology in semiconductor device fabrication is used to determine how well one printed layer is overlaid on a previously printed layer. Close alignment of each layer at all points within the device is crucial for reaching the design goals and hence the required quality and performance of the manufactured device. It is consequently of importance for the efficiency of the manufacturing process that any alignment error between two patterned layers on a wafer, especially successive patterned layers can be measured accurately. It is similarly important to be able to measure any alignment error between successive exposures in the same layer, and where reference is made herein for convenience to two layers it will be understood where appropriate to apply equally to two exposures in the same layer.

Misregistration between layers is referred to as overlay error. Overlay metrology tools are used to measure the overlay error. This information may be fed into a closed loop system to correct the overlay error.

Current overlay metrology employs optically readable target patterns, printed onto the successive layers of a semiconductor wafer during fabrication. The relative displacement of two successive layers is measured by imaging the patterns at high magnification, digitizing the images, and processing the image data using various known image analysis algorithms to quantify the overlay error.

The pattern of the target mark may be applied to the wafer by any suitable method. In particular, it is often preferred that the mark is printed onto the wafer layers using photolithographic methods. Typically, the same technique is used to apply overlay target marks on each of two wafer layers to be tested to enable alignment information to be measured which is representative of the alignment of the layers. Accuracy of layer alignment should correspond to accuracy of circuit pattern alignment within the fabricated wafer.

Current overlay metrology is normally practised by printing targets with rectangular symmetry. For each measurement two targets are printed, one in the current layer and one in a previous layer, or one in association with each pattern in a common layer. The choice of which previous layer to use is determined by process tolerances. The two targets have a nominally common centre, but are printed with different sizes so that they can be differentiated. Normally, but not always, the target printed in the current layer is the smaller of the two targets. An overlay measurement in such a system is the actual measured displacement of the centres of the two targets.

Current preferred practice is that the size of the targets is designed such that both can be imaged simultaneously by a bright-field microscope. Imaging considerations determine that the larger of the two targets is typically a 25μm square on the outside. This arrangement permits capture of all of the necessary data for the performance of the measurement from a single image.

Measurements at a rate of one in every two seconds or less are possible using current technology.

The procedure necessarily requires that the target and its image are symmetric, since otherwise there is no uniquely defined centre point. Without symmetry there is an uncertainty in the measurement, which may be more than can be tolerated. Within that general requirement, optimal sizes and shapes of current designs of targets to be measured are well known. The targets are positioned in the scribe area at the edge of the fabricated circuit.

It is generally highly desirable that the measurement targets maintain axial symmetry about the optical axis of the measurement tool, since accurate measurement requires very close control of image aberrations and this can only be achieved in practice for images at or centred about the system axis. In most prior art systems, measurements are therefore made from the targets by computing a centre line for each different target. The overlay measurement is the difference in the centre lines. Most of the target designs in general use permit measurement of the vertical and horizontal overlay displacement from a single image.

Measurement errors must be controlled to a very small amount. Errors known to arise are classified as random errors, characterized by determination of measurement precision; and systematic errors, characterized by tool induced errors, tool-to-tool measurement differences and errors introduced by asymmetry in the targets being measured. Successful application of overlay metrology to semiconductor process control is generally held to require that, combined, these errors are less than 10% of the process control budget. This measurement error budget is in practice in the range 1 to 5 nm, and will remain so in the foreseeable future.

Measurement precision is easily determined by analysis of the variations of repeated measurements. Different forms of precision may be determined by well known appropriate methods, allowing determination of the static, short-term and long-term components of precision.

Determining the contribution of the measurement tool alone to errors is achieved by comparing measurements made with the target in its normal presentation with a measurement made after rotating the target by 180° with respect to the imaging system. Ideally the measurement will simply change sign. The average of the measurements at 0° and 180° is called *Tool Induced Shift* (TIS), as is well known to those skilled in the art, and is widely accepted as a measure of the tool's systematic error contribution. Measurements of TIS differ from tool to tool and with process layer. Subtraction of the estimated TIS error from the measurements allows removal of the TIS error from the measurements, but at the expense of the additional time taken to measure the target twice.

Different tools, even when of the same type, will make slightly different measurements, even after allowing for precision and TIS errors. The magnitude of this error can be determined experimentally by comparing the averages of repeated measurements at 0° and 180° on two or more tools.

The contributions of precision, TIS and tool-to-tool differences are normally combined through a root-sum-square product, or alternative appropriate method, to determine the total measurement uncertainty due to the measurement process. The total measurement uncertainty must be less than 10% of the overall overlay budget for the process if the metrology is to have value. Existing measurement tools and procedures achieve a total uncertainty within that required for current process technologies but insufficient for future requirements.

By contrast, although the contribution of asymmetry in the measurement target itself is widely understood it is not normally determined. It is known that in many cases it can be much larger than the tool contribution to measurement uncertainty. There are two sources of error to be considered:

1. Imperfection in the manufacture of the target which leads to an uncertainty in its location. An example of this is physical asymmetry of the target, caused perhaps by uneven deposition of a metal film.
2. Difference in the displacement of the two layers at the measurement target and the genuine overlay of the same layers in the device being manufactured. These can arise from errors in the design and manufacture of the reticles used to create the patterns on the wafer, proximity effects in the printing process and distortion of the films after printing by other process steps.

These measurement errors represent a practical limitation of the current state of the art which causes severe problems in the application of overlay metrology to semiconductor process control.

Improvements to the first of these problems can sometimes be achieved by fabricating the features in the measured targets from much smaller objects - lines or holes. These smaller features are printed at the design rule for the process, currently in the range 0.1-0.2 μm, and are grouped close together. They are too small to be individually resolved by the optical microscopes used in overlay metrology tools. The small features are grouped into larger shapes in the pattern of traditional overlay targets. The use of small features avoids some of the mechanisms causing imperfections in the shape of the manufactured targets, in part by taking advantage of the optimization of the manufacturing process for objects of this size and shape.

A further problem is introduced by the size of the targets, which are a significant fraction of the space available in the scribe area surrounding the devices being fabricated. It is desired that the size of these areas be reduced, which means that it is also highly desirable that the measurement targets be made smaller. However, the size of the target cannot be reduced too much, since accurate measurement requires that the measured features are not significantly smaller than the resolution of the microscope system, and achieving good precision requires that as many as possible of such features are visible in the image.

It has been shown (Smith, Nigel P.; Goelzer, Gary R.; Hanna, Michael; Troccolo, Patrick M., "*Minimizing overlay measurement errors*", August 1993, Proceedings of SPIE Volume: 1926 Integrated Circuit Metrology, Inspection, and Process Control VII, Editor(s): Postek, Michael T) that space must be left between the features printed from the two layers else the proximity of one to another causes an error in the measurement. The magnitude of this error depends on the resolution of the imaging microscope system, but must be 5 μm or greater in practical designs if the measurement error is to be contained within practical limits. This proximity effect further limits the extent to which the size of the targets can be reduced.

However, high speed is one of the key advantages of existing overlay metrology practice, and any process development must not lose this advantage if it is to be viable in production use. This requirement means that uncertainty reduction by the use of repeated measurements is highly undesirable. There is thus a general desire to develop alternative overlay patterns and/or analysis methods which apply the basic principles of existing metrologies but in a manner that mitigates some or all of these errors to produce an improved fabrication metrology, and in particular a metrology offering improved accuracy without substantial loss of throughput speed.

In accordance with the present invention in a first aspect an overlay mark for determining the relative position between two or more layers of a semiconductor structure or between two or more separately generated patterns on a single layer of a semiconductor structure comprises a first mark portion associated with a first layer or pattern as the case may be and a second mark portion associated with a second layer or pattern as the case may be, wherein each mark portion comprises a single two dimensional generally orthogonal, and preferably generally square, array of individual test structures.

The invention discloses novel target designs that address the disadvantages of the existing technology, in particular offering significantly improved accuracy, without sacrificing advantages in relation to speed of processing and otherwise.

The invention exploits the realisation that effective information about alignment in two directions may be given by a single square array exploiting entirely conventional imaging techniques, such as the bright field techniques commonplace in the prior art. Scanning this pattern in two dimensions, more specifically orthogonal X-Y scanning parallel to the two linear directions of the array, yields information about misalignment in both directions. This offers the potential to yield an overlay error measurement representative of layer or pattern misalignment in two dimensions from a single marked region using standard or specifically developed image analysis techniques to determine the misregistration between the two patterns. More complex patterns involving two or more regions in each mark, each adapted to measure misalignment in a particular direction, are not necessary, provided a single accurately disposed array of individual test structures in accordance with the invention is laid down upon each layer, or associated with each pattern, as the case may be.

A further advantage is that existing metrology tools may be simply adapted to their measurement, avoiding the costs involved in retooling that radically different methods would require.

Each mark portion is spatially associated with a layer or pattern under test, so that the measured overlay error is representative of the misalignment between the respective layers or patterns. Overlay marks in accordance with the invention are equally suited to measurement of alignment errors between layers, in particular but not limited to consecutive layers, and alignment error between different exposures in the same layer, and where reference is made herein for convenience to two layers it will be understood where appropriate to apply equally to two exposures in the same structural layer. Where the overlay mark is used to aid measurement of alignment between different layers, the first mark portion is laid down upon a first layer, in particular an uppermost layer, and the second mark portion is laid down upon a second layer below the said first layer, such that the test structures of the second layer are detectable through the first layer. The uppermost mark portion serves as an alignment marking, and the lower mark portion as the reference marking.

The test structures comprising each mark portion are disposed in each case as a single two dimensional array with an orthogonal arrangement. This should be understood to mean that each array comprises an arrangement of individual test structures forming a plurality of parallel rows and columns, the row and column directions being at right angles to each other. In use these should correspond to the mirror angles of the optical equipment used for image analysis. For most applications a substantially square array, with generally constant spacing between test structures throughout the array, will be preferred. In certain cases, a functionally varying spacing between adjacent rows and/or columns respectively in a column/ row direction as the case may

be might be useful for particular functionality, provided always that the orthogonal relationship of rows and columns is maintained.

Preferably the spacing between test structures in the array comprising the first mark portion and the spacing between test structures in the array comprising the second mark portion is equivalent. In particular both are square arrays of generally equal spacing.

The overall mark portion preferably also has a generally square outline. It is desirable if asymmetries are to be avoided. However minor deviations in particular are unlikely to be significant. Moreover, the requirement for an orthogonal array of successive rows and columns does not preclude designs where individual test structures are absent from a limited portion of the sites defined thereby. Such gaps might be incorporated for example to add readable information, or to include further mark features giving such give additional information. Such gaps/ additional marks are preferably located so as to maintain symmetry of the structure in the mark portion and/ or about the intended optic axis of the imaging apparatus.

The dimensions of each test structure within each array and the spacing thereof will be optimally determined by and are therefore preferably set with reference to the resolution limit of the imaging microscope. Typically therefore each test structure will have a width of around 0.5 to 2 μm. Spacing between test structures in the array will preferably be between one and four structure widths. This will maximise feature density at the resolution limit of the imaging device. Any specific design embodying the principles of the invention will increase the number of feature transitions when compared with many previous designs. Each array may comprise several test structures in each direction, preferably at least five, while fitting comfortably into a

conventional mark area. The additional image detail provides more information content in the image, providing for an improvement in measurement precision.

The individual test structures making up each array are preferably substantially identically sized and shaped. Each test structure conveniently has generally square geometry.

Individual test structures may optionally be made using design rule sized sub-structures to address issues of process induced inaccuracy, as is well known. Suitable arrangements, familiar to those skilled in the art, include parallel arrays of elongate rectangular sub-structures in either direction, arrays of square sub-structures, circles in square or hexagonal array, arrays of holes within a suitably shaped test structure and any combinations of these or other like patterns. Sub-structure dimensions are set by design rule limits, being typically for present techniques of the order of 100 to several hundreds of nanometres. However advances in manufacturing processes are likely to further reduce these dimensions in the future.

In use with a standard imaging device, the orthogonal arrays making up each mark portion are to be aligned with the vertical and horizontal grid directions of each array (ie the rows and columns formed by the test structures) parallel to each other and to the X-Y symmetry lines of the imaging device. It has been noted that optimal performance depends on measurement being centred on the optic axis of the imaging device. Two embodiments are proposed to facilitate this.

In a first embodiment the arrays of test structures making up the first and second mark portions are disposed such that the first portion overlays the second portion and that the test structures of second portion are arrayed within

the gaps between the test structures of the first portion and visible therebetween. In particular, each test structure in the second portion is located at a point sitting at the diagonal centre of a square bounded at each corner by test structures of the first portion.

Preferably, the two test portions are laid down with generally co-located centres, the common centre intended to correspond to the optic axis of the imaging system in use, but it will be understood that minor asymmetry in this regard, especially at the edges of the structure will not seriously degrade measurement accuracy as long as the interlaced arrangements is maintained.

In this embodiment, the design is optimised if test structures in each array are spaced with a periodicity around three to four times the width of an individual test structure. This provides adequate gaps in the array comprising the upper mark portion for visibility of test structures in the lower mark portion therethrough.

In a second embodiment the test structures making up the first and second mark portions are disposed such that the first portion is laterally spaced from the second portion in a spacing direction parallel to a horizontal or vertical direction of the square arrays such that a notional line in the spacing direction can be drawn about which each array exhibits mirror symmetry. In use this will correspond to one of the mirror axes of the imaging device, with the centre point of this notional line equidistant from each mark portion intended to correspond to the optic axis of the imaging system. Each mark portion will preferably comprise an identical pattern of test structure.

In this embodiment, the design is optimised if test structures in each array are spaced with a periodicity of two to three structure widths, in particular around

two, i.e. so that the spacing between test structures is the same as the width of an individual structure.

The test structures making up the array comprising each mark portion may be laid down by any suitable technique known to those skilled in the art, in particular the photolithographic techniques above described.

The advantages of existing target designs are retained. The measurements are made from a single image so that speed is not compromised. The measurement is made using an optical image, so that existing imaging tools can be used. Overlay error may be quantified using any suitable known or specifically developed image processing technique.

Thus, in accordance with the present invention in a second aspect a method for providing an overlay mark to determine the relative position between two or more layers of a semiconductor structure or between two or more separately generated patterns on a single layer of a semiconductor structure comprises the steps of:

laying down a first mark portion in association with a first layer or pattern as the case may be;

and laying down a second mark portion in association with a second layer or pattern as the case may be;

wherein each mark portion comprises a single two dimensional generally square array of generally evenly spaced individual test structures.

Similarly, in accordance with the present invention in a third aspect a method for determining the relative position between two or more layers of a semiconductor structure or between two or more separately generated patterns on a single layer of a semiconductor structure comprises the steps of:

laying down a first mark portion in association with a first layer or pattern as the case may be;

laying down a second mark portion in association with a second layer or pattern as the case may be; wherein each mark portion comprises a single two dimensional generally square array of generally evenly spaced individual test structures;

optically imaging the two mark portions in a horizontal and vertical array direction;

collecting and digitizing the image;

numerically analysing the digitized data to obtain a quantified measurement of the misalignment of the first and second mark portions.

Each mark portion is preferably laid down by a photolithographic process. Optical imaging of the mark is preferably carried out using bright field microscopy. Other preferred features of the methods will be understood by analogy with the foregoing.

The invention will now be described by way of example only with reference to figures 1 to 2 of the accompanying drawings, in which:

Figure 1 is a general schematic of a mark in accordance with a first principal embodiment of the invention comprising superimposed mark portions;

Figure 2 is a general schematic of a mark in accordance with a second principal embodiment of the invention comprising adjacent mark portions;

In all of the figures, the mark comprises a first or alignment mark portion on a first layer or associated with a first pattern on a common layer, and a second or reference mark portion on a second lower layer or associated with a second lower pattern on a common layer. The first mark portion is represented by

lighter grey-shaded structures. The second mark portion, configured to be at least partially visible in conjunction with the first, is represented by darker grey-shaded structures.

In each case the invention lies in the arrangement of periodic test structures. The periodic structures and any sub-structures making up the test structures are formed using any suitable processes. Typically these will include lithographic processes that are generally known in the art. Misalignment is measured using imaging systems and image analysis techniques, which may be standard systems and techniques that are generally known in the art or systems and techniques modified to be optimized specific to the marks in accordance with the invention.

Figure 1 illustrates a top plan view of an alignment mark according to one embodiment of the invention. The mark is shown in the intended configuration that results when the tested layers of a structure are in proper alignment. The mark consists of two mark portions, one on each layer, comprising substantially identical square arrays of test structures overlaid into an interlocking pattern, whereby the test structures of the second mark portion lie at the centres of notional squares bounded at the corners by test structures in the first mark portion.

Each array also has an overall square shape. The two arrays are laid down with a common centroid. The first mark portion is larger by one pattern repeat in both directions, and offset relative to the second by half a pattern repeat in both directions, to maintain rotational symmetry about the common centroids. This common centroid should correspond to the optic axis of the imaging system in use, with mirror axes of the imaging system parallel to the rows and columns of the squares. Given appropriate axis orientation of a suitable imaging device the rows in each array may serve for x-axis registration

measurements and the columns for y-axis registration measurements. The simple mark, with a single array comprising the mark portion on a layer, can thus give two dimensional registration information.

Each of the mark portions consists of a square array of periodic test structures. Each of the test structures in the example is also square in general outline. Each is shown solid in this plan view, but it will be well understood that it could comprise multiple sub-structures at a design rule level (examples of which are given below) for reasons that will be familiar. In a specific implementation of the example mark each test structure comprises a 1 μm square. Lateral spacing between squares is then around 3 μm to provide the necessary gaps for the interlocking arrangement of the two arrays. Dimensions are set to maximise feature density within a normal mark area and hence accuracy, subject to the resolution limit of a typical imaging system. The measurements will vary in practice, depending on the required accuracy and the resolution limit of the imaging system.

A gap is provided in the centre of the array, into which an identification key mark could be included with the overlay layer to ensure that correct reference and overlay are matched. This is optional. Alternatively, the arrays may be continuous across the centre.

Figure 2 illustrates a top plan view of an alignment mark according to a second embodiment of the invention. The mark is shown in the intended configuration that results when the tested layers of a structure are in proper alignment. The mark consists of two mark portions, one on each layer, comprising substantially identical square arrays of test structures. Each array also has an overall square shape.

The two arrays are laid down displaced apart about a notional line which can be drawn parallel to the array rows so as to form a notional mirror symmetry line for each square. The centre of this notional line should correspond to the optic axis of the imaging system in use, with mirror axes of the imaging system parallel to the rows and columns of the squares. As before, with appropriate axis orientation of a suitable imaging device the rows in each array may serve for x-axis registration measurements and the columns for y-axis registration measurements so that the simple mark, with a single array comprising the mark portion on a layer, can give two dimensional registration information.

Each of the mark portions consists of a square array of periodic test structures. As before, each of the test structures in the example is also square in general outline and shown solid but could comprise multiple sub-structures at a design rule level. In a specific implementation of the example mark each test structure comprises a 1 μm square. Lateral spacing between squares is also around 1 μm. Dimensions are again set to maximise feature density subject to the resolution limit of a typical imaging system.

Figure 1

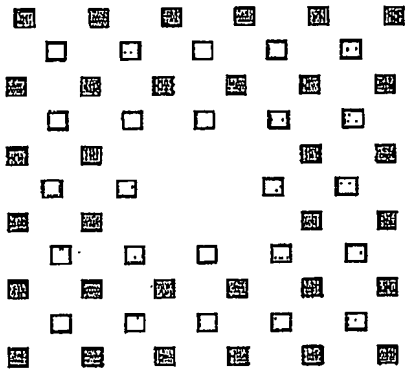
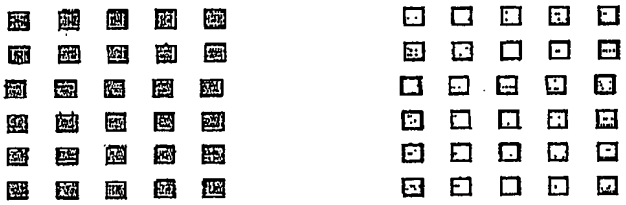


Figure 2.



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